**Question 12 pts**

**Part 1: Functional Completeness**

Simulate the circuit diagram P0Gates. Determine the output for each set of input cases, and complete each truth table using your observations. Then identify each gate based on the truth table you complete.

Complete the truth table for the circuit whose output is F1. For each value of input A, place a "0" or a "1" in the blank to indicate the value of output F1.

| **Input A** | **Output F1** |
| --- | --- |
| 0 |  |
| 1 |  |

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**Question 24 pts**

The circuit whose output is F1 represents which of these logic gates?

|  |  |
| --- | --- |
|  | NOT gate / inverter |
|  | AND gate |

|  |  |
| --- | --- |
|  | OR gate |
|  | NAND gate |

|  |  |
| --- | --- |
|  | NOR gate |
|  | XOR gate |

|  |  |
| --- | --- |
|  | XNOR gate |

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**Question 34 pts**

Complete the truth table for the circuit whose output is F2. For each combination of inputs A and B, place a "0" or a "1" in the blank to indicate the value of output F2.

| **Input A** | **Input B** | **Output F2** |
| --- | --- | --- |
| 0 | 0 |  |
| 0 | 1 |  |
| 1 | 0 |  |
| 1 | 1 |  |

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**Question 44 pts**

The circuit whose output is F2 represents which of these logic gates?

|  |  |
| --- | --- |
|  | NOT gate / inverter |
|  | AND gate |

|  |  |
| --- | --- |
|  | OR gate |
|  | NAND gate |

|  |  |
| --- | --- |
|  | NOR gate |
|  | XOR gate |

|  |  |
| --- | --- |
|  | XNOR gate |

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**Question 54 pts**

Complete the truth table for the circuit whose output is F3. For each combination of inputs A and B, place a "0" or a "1" in the blank to indicate the value of output F3.

| **Input A** | **Input B** | **Output F3** |
| --- | --- | --- |
| 0 | 0 |  |
| 0 | 1 |  |
| 1 | 0 |  |
| 1 | 1 |  |

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**Question 64 pts**

The circuit whose output is F3 represents which of these logic gates?

|  |  |
| --- | --- |
|  | NOT gate / inverter |
|  | AND gate |

|  |  |
| --- | --- |
|  | OR gate |
|  | NAND gate |

|  |  |
| --- | --- |
|  | NOR gate |
|  | XOR gate |

|  |  |
| --- | --- |
|  | XNOR gate |

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**Question 74 pts**

Complete the truth table for the circuit whose output is F4. For each combination of inputs A and B, place a "0" or a "1" in the blank to indicate the value of output F4.

| **Input A** | **Input B** | **Output F4** |
| --- | --- | --- |
| 0 | 0 |  |
| 0 | 1 |  |
| 1 | 0 |  |
| 1 | 1 |  |

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**Question 84 pts**

The circuit whose output is F4 represents which of these logic gates?

|  |  |
| --- | --- |
|  | NOT gate / inverter |
|  | AND gate |

|  |  |
| --- | --- |
|  | OR gate |
|  | NAND gate |

|  |  |
| --- | --- |
|  | NOR gate |
|  | XOR gate |

|  |  |
| --- | --- |
|  | XNOR gate |

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**Question 94 pts**

**Part 2: Bubble Propagation**

Simulate the circuit diagram P0Bubble. Use the circuits to answer the questions below. Then determine the output for each set of input cases and complete each truth table using your observations.

Complete the truth table for the circuit whose output is G1. For each combination of inputs P and Q, place a "0" or a "1" in the blank to indicate the value of output G1.

| **Input P** | **Input Q** | **Output G1** |
| --- | --- | --- |
| 0 | 0 |  |
| 0 | 1 |  |
| 1 | 0 |  |
| 1 | 1 |  |

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**Question 104 pts**

The circuit whose output is G1 represents which of these logic gates?

|  |  |
| --- | --- |
|  | NOT gate / inverter |
|  | AND gate |

|  |  |
| --- | --- |
|  | OR gate |
|  | NAND gate |

|  |  |
| --- | --- |
|  | NOR gate |
|  | XOR gate |

|  |  |
| --- | --- |
|  | XNOR gate |

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**Question 111 pts**

Compare the value of output G2 to the value of input X. Does inverting a signal twice affect the signal's value?

|  |  |
| --- | --- |
|  | Yes |
|  | No |

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**Question 124 pts**

Which of your Boolean algebra axioms expresses this fact?

|  |  |
| --- | --- |
|  | x + 0 = x |
|  | x • 1 = x |

|  |  |
| --- | --- |
|  | x + 1 = 1 |
|  | x • 0 = 0 |

|  |  |
| --- | --- |
|  | x + x = x |
|  | x • x = x |

|  |  |
| --- | --- |
|  | x + x' = 1 |
|  | x • x' = 0 |

|  |  |
| --- | --- |
|  | (x')' = x |
|  | x + y = y + x |

|  |  |
| --- | --- |
|  | xy = yx |
|  | x + (y + z) = (x + y) + z |

|  |  |
| --- | --- |
|  | x(yz) = (xy)z |
|  | x(y + z) = xy + xz |

|  |  |
| --- | --- |
|  | x + yz = (x + y)(x + z) |
|  | (x + y)' = x'y' |

|  |  |
| --- | --- |
|  | (xy)' = x' + y' |

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**Question 134 pts**

Complete the truth table for the circuit whose output is G3. For each combination of inputs P and Q, place a "0" or a "1" in the blank to indicate the value of output G3.

| **Input P** | **Input Q** | **Output G3** |
| --- | --- | --- |
| 0 | 0 |  |
| 0 | 1 |  |
| 1 | 0 |  |
| 1 | 1 |  |

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**Question 144 pts**

The circuit whose output is G3 represents which of these logic gates?

|  |  |
| --- | --- |
|  | NOT gate / inverter |
|  | AND gate |

|  |  |
| --- | --- |
|  | OR gate |
|  | NAND gate |

|  |  |
| --- | --- |
|  | NOR gate |
|  | XOR gate |

|  |  |
| --- | --- |
|  | XNOR gate |

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**Question 154 pts**

The circuit whose output is G3 was derived using bubble propagation. Which of these gates is equivalent to "*an OR gate that has all of its inputs inverted*"?

|  |  |
| --- | --- |
|  | NOT gate / inverter |
|  | AND gate |

|  |  |
| --- | --- |
|  | OR gate |
|  | NAND gate |

|  |  |
| --- | --- |
|  | NOR gate |
|  | XOR gate |

|  |  |
| --- | --- |
|  | XNOR gate |

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**Question 164 pts**

Which of your Boolean algebra axioms expresses this fact?

|  |  |
| --- | --- |
|  | x + 0 = x |
|  | x • 1 = x |

|  |  |
| --- | --- |
|  | x + 1 = 1 |
|  | x • 0 = 0 |

|  |  |
| --- | --- |
|  | x + x = x |
|  | x • x = x |

|  |  |
| --- | --- |
|  | x + x' = 1 |
|  | x • x' = 0 |

|  |  |
| --- | --- |
|  | (x')' = x |
|  | x + y = y + x |

|  |  |
| --- | --- |
|  | xy = yx |
|  | x + (y + z) = (x + y) + z |

|  |  |
| --- | --- |
|  | x(yz) = (xy)z |
|  | x(y + z) = xy + xz |

|  |  |
| --- | --- |
|  | x + yz = (x + y)(x + z) |
|  | (x + y)' = x'y' |

|  |  |
| --- | --- |
|  | (xy)' = x' + y' |

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**Question 171 pts**

Compare the behaviors of the circuits whose output is G3 to the output of the circuit whose output is G4. Does changing the invert-OR gate into its equivalent - the one you identified in Question 15 - change the function's output behavior?

|  |  |
| --- | --- |
|  | Yes |
|  | No |